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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/790,509
Filing Date: March 01, 2004
Appellant(s): AHLUWALIA, MANISH K.

Karen G. Hazzah
(Reg. No. 48,472)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/20/2009 appealing from the Office action mailed 4/29/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,907,494	ARIMILLI et al.	6-2005
6,918,023	BROWNING etal.	7-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 23, the newly amended limitation "a computer readable storage medium" is not properly defined in the specification. It appears that the specification merely define a computer readable medium may include any medium that can store or transfer

information (see page 7 line 8-21). The original specification fails to clearly define or describe what "a computer readable storage medium" is in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over (US PAT. 6,907,494 hereinafter Armilli) in view of Browning et al. (US PAT. 6,918,023 hereinafter Browning).

Regarding claim 1, Armilli discloses a computer device (8, figure 3) comprising a processor (10, figure 3), a memory (22, figure 3) coupled to the processor via the system bus (12, figure 3), and program instructions provided to the memory and executable by the processor to track a virtual address space for a process associated with a device connected to the computer device (figure 2 and col. 5 line 66 through col. 6 line 39), and release a physical address space associated with the virtual address space when the device has a connection removed from the computer device (col. 7 lines 32-57, i.e., removing memory module from data processing system). Armilli differs from the claimed invention in not specifically teaching to provide an

indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid for use by the process, wherein the indication is triggered by detection that he physical address space that was being used by processes associated with the device has been released; and wherein the indication occurs responsive to the physical address space being released and before release of the virtual address space by the process. However, Browning teaches a method for invalidating specified pre-translations maintained in a data processing system which maintains decentralized copies of pre-translations, wherein the data processing system comprising a DMA mapping agent to map a virtual buffer to physical address (steps 802-816, figure 8), when a detection on memory removal operation is being process (col. 7 lines 21 through col. 8 line 44), and also defined in figure 8 that determining whether the RPN entry for the virtual memory page is valid (step 824), when flag is set on memory removal process (step 834), i.e., the indication is triggered by detection that the physical address space that was being used by process associated with the device is being released, and the virtual memory page is maintained for mapping as defined in step 828, and further comprising the steps of to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, as defined in steps 824-830 in figure 8, and (step 910, figure 9 and col. 8 lines 58-64, i.e., scan all registered RPN lists and invalidates all entries, including virtual address space, corresponding to real pages that within the range of memory to be removed), and (col. 8 lines 53-58, i.e., receiving acknowledgement of interrupt from all CPUs and then triggering to register by detecting that real pages that are within range of memory to be removed). Therefore, it would have been obvious to a person of ordinary skill in the art at the

time the invention was made to modify Arimilli to provide an indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid for use by the process, wherein the indication is triggered by detection that he physical address space that was being used by processes associated with the device has been released; and wherein the indication occurs responsive to the physical address space being released and before release of the virtual address space by the process, as per teaching of Browning, in order to provide for invalidating pre-translations without the use of locks or semaphores.

Regarding claims 2-3, Arimilli discloses the device includes a device, i.e., mapping engine (26, figure 3), which can be mapped to memory, and the virtual address space includes an input/output space (col. 7 lines 58-65).

Regarding claim 4, Arimilli discloses the program instructions are part of a memory management system, which includes a virtual memory data structure associated with the process (col. 6 line 66 through col. 7 line 15).

Regarding claim 5, Arimilli discloses the program instructions execute to register the virtual address space is no longer valid for process use in the virtual memory data structure associated with the process (col. 8 lines 9-26).

Regarding claim 6, Arimilli discloses the program instructions execute to allocate the virtual address space when the process requests physical memory (col. 8 line 51 through col. 9 line 10).

Regarding claim 7, Arimilli discloses the program instructions execute to register that the virtual address space is available for use when the process releases the virtual address space (col. 7 lines 32-57).

Regarding claim 8, Arimilli discloses a computing device (8, figure 3) comprising a processor (10, figure 3), a random access memory (22, figure 3) coupled to the processor via the system bus (12, figure 3), and program instructions provided to the memory and executable by the processor to deference a virtual address space for a process associated with a removable memory mappable device connected to the computer system (figure 2 and col. 5 line 66 through col. 6 line 39), and release a physical address space associated with the virtual address space when the device has a connection removed from the computer device (col. 7 lines 32-57). Although Armilli teaches to register that the virtual address space before when the process has released the virtual address space (col. 7 lines 32-42), Armilli differs from the claimed invention in not specifically teaching to register by providing an indication in a virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use subsequent to when the physical address space is released, wherein registering is triggered by detection that he physical address space that was being used by processes associated with the device has been released; and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process. However, Browning teaches a method for invalidating specified pre-translations maintained in a data processing system which maintains decentralized copies of pre-translations, wherein the data processing system comprising a DMA mapping agent to map a virtual buffer to physical address (steps 802-816, figure 8), when a detection on memory removal operation is being

process (col. 7 lines 21 through col. 8 line 44), and also defined in figure 8 that determining whether the RPN entry for the virtual memory page is valid (step 824), when flag is set on memory removal process (step 834), i.e., registering is triggered by detection that the physical address space that was being used by process associated with the device is being released, and the virtual memory page is maintained for mapping as defined in step 828, and further comprising the steps of to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, as defined in steps 824-830 in figure 8, and (step 910, figure 9 and col. 8 lines 58-64, i.e., scan all registered RPN lists and invalidates all entries, including virtual address space, corresponding to real pages that within the range of memory to be removed), and (col. 8 lines 53-58, i.e., receiving acknowledgement of interrupt from all CPUs and then triggering to register by detecting that real pages that are within range of memory to be removed). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Arimilli to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, wherein registering is triggered by detection that he physical address space that was being used by processes associated with the device has been released; and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process, as per teaching of Browning, in order to provide for invalidating pre-translations without the use of locks or semaphores.

Regarding claim 9, Arimilli discloses the program instructions execute to un-map the virtual address space in a manner which does not violate semantics for an operating system of the computing device (abstract and col. 11 lines 6-26).

Regarding claim 10, Arimilli differs from the claimed invention in not specifically teaches the operating system is selected from the group of a Unix operating system and a Linux operating system. However, it is old and notoriously well know in the art that kernel is a core of an operating system, a portion of the system that manages memory, files, and peripheral devices, maintains the time and data, launches applications, and allocates system resources, as defined by *Microsoft Computer dictionary Fifth edition*, furthermore, kernel is defined as an operating system (OS) of the essential part of Unix operating systems, i.e., Linus OS in *On-line Computing Dictionary* (http://www.instantweb.com/foldoc/foldoc.cgi?query=kernel&action=Search). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the operating system in the computer system of Arimilli is selected from the group of a Unix operating system and a Linux operating system, because it improves and enhances the flexibility in the computer system.

Regarding claims 11-12, Arimilli discloses the program instructions execute to allow the process to un-map the virtual address space subsequent to the release of the physical address space and to indicate an operation as failed if the process attempts to perform the operation subsequent to registering that the virtual address space is no longer valid for process use (col. 7 lines 17-42).

Regarding claim 13, Armilli discloses a computer device (8, figure 3) comprising a processor (10, figure 3), a memory (22, figure 3) coupled to the processor via a system bus (12,

figure 3), the memory including program instructions for maintaining a virtual memory data structure specific to a process as part of a memory management system, i.e., program provided an address translation mechanism that translates virtual addresses to physical addresses (col. 5 lines 5-53), and means for un-mapping a virtual address space, i.e., processor's move engine (28, figure 3), for a process in a manner which does not violate semantics for an operating system of the computing device when a removable memory mappable device associated with the process is logically disconnected (abstract and col. 7 line 32 through col. 9 line 10, i.e., the processor's move engine works in conjunction with the associated mapping engine to take the associated memory module offline, read as un-mapping a virtual address space, prior to its physically removal, read as when the removable memory mappable device associated with the process is logically disconnected, such that the memory module can be removed in physical memory without the operating system having to direct and control the reconfiguration of physical memory to accomplish the physical memory chance, read as for a process in a manner which does not violate semantics for an operating system of the computing device). Arimilli differs from the claimed invention in not specifically teaching that means for un-mapping the virtual address space for the process that is triggered as a physical address space used by the process is being released. However, Browning teaches a method for invalidating specified pre-translations maintained in a data processing system which maintains decentralized copies of pre-translations, wherein the data processing system comprising a DMA mapping agent to map a virtual buffer to physical address (steps 802-816, figure 8), when a detection on memory removal operation is being process (col. 7 lines 21 through col. 8 line 44), and also defined in figure 8 that determining whether the RPN entry for the virtual memory page is valid (step 824), when flag is

set on memory removal process (step 834), i.e., registering is triggered by detection that the physical address space that was being used by process associated with the device is being released, and the virtual memory page is maintained for mapping as defined in step 828, and further comprising the steps of to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, as defined in steps 824-830 in figure 8, and (step 910, figure 9 and col. 8 lines 58-64, i.e., scan all registered RPN lists and invalidates all entries, including virtual address space, corresponding to real pages that within the range of memory to be removed), and (col. 8 lines 53-58, i.e., receiving acknowledgement of interrupt from all CPUs and then triggering to register by detecting that real pages that are within range of memory to be removed). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Arimilli in having means for un-mapping the virtual address space for the process that is triggered as a physical address space used by the process is being released, as per teaching of Browning, in order to provide for invalidating pre-translations without the use of locks or semaphores.

Regarding claim 14, Arimilli discloses the program instructions execute to dereference the virtual address space for the process (col. 7 line 43 through col. 8 line 8 line 50, i.e., to perform memory reconfiguration in response to memory module M2 being removed from data processing system).

Regarding claim 15, Arimilli discloses the means for un-mapping the virtual address space includes program instructions, which execute to maintain a representation of an object associated with the process in the virtual memory data structure of the process (col. 8 line 51

through col. 9 line 10, i.e., creating a virtualized physical mapping from the addressable read address space being utilized by operating system into a virtual physical address space).

Regarding claim 16, Browning discloses the means for un-mapping the virtual address space includes program instructions which execute to remove a mapping of the object to physical memory (col. 8 line 45 through col. 9 line 27).

Regarding claims 17-18, Browning discloses the means for un-mapping the virtual address space includes program instructions which execute to register in the virtual memory data structure of the process that the virtual address space associated with the process is not available for use, and the program instructions execute to set a bit in the region of the virtual memory data structure to indicate that the virtual address space is not available for use (col. 8 line 45 through col. 9 line 27).

Regarding claim 19, the limitations of the claim are rejected as the same reasons as set forth in claim 8.

Regarding claims 20-21, the limitations of the claims are rejected as the same reasons set forth in claims 11-12.

Regarding claim 22, the limitations of the claim are rejected as the same reasons as set forth in claim 1.

Regarding claim 23, the limitations of the claim are rejected as the same reasons set forth in claim 19.

(10) Response to Argument

Appellant's arguments filed 7/20/2009 have been fully considered but they are not persuasive.

A. Rejection of claim 23 under 35 U.S.C. § 112, ¶ 1 (written description)

1. In response to Appellant's argument that the *prima facie* case is insufficient, examiner respectfully disagreed because appellant admitted in Appeal Brief (page 8) that the instant specification *only* defines computer readable medium as including any medium that can store or transfer information such that the instant specification fails to define the claimed limitation "computer readable storage medium". Thus, examiner submits that the *prima facie* case for a written description is sufficient, and the rejection is maintained.

2. In response to Appellant's argument that the specification does reasonable convey possession of a "computer readable storage medium" because the term is clearly understood, as a matter of plain English, to be a particular type of computer readable medium, one that stores computer readable instructions. In fact, the specification specifically supports this understanding: "A computer readable medium may include any medium that can store or transfer information." (para. 0024.), Examiner respectfully disagrees because it is notoriously well known in the art that computer readable medium is a broad term in accordance with plain meaning that includes any type of memory devices, as well as signals or carrier waves such that any type of memory devices, as well as signals or carrier waves can store and transfer information. Note the instant specification does not specifically define "computer readable storage medium. Thus, one

skilled artisan would not have understood the inventor to be in possession of the claimed invention at the time of filing.

3. In response to Appellant's argument that the Examiner unfairly replaced a § 101 rejection with a § 112, ¶1 (written description) rejection, it is noted that examiner does not replace a § 101 rejection with a § 112, ¶1 (written description) rejection. In fact, examiner identified the issue in accordance with appellant's response filed 2/17/2009. As further reviewed the prosecution history, it found that the amended limitation "computer readable storage medium" was not defined in the instant specification.

4. Conclusion

For at least these reasons, the rejection under § 112, ¶1 written description is proper, and the rejection should be sustain.

B. Rejection of Claims 1-23 under 35 U.S.C. § 103(a): Armilli and Browning et al.

Examiner submits that a prima facie case of obviousness for claims 1-23 has been established using the references of the record, for at least the following reasons:

1. Independent claim 1

a. The proposed combination does not teach " providing an indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid for use by the process"

(1) RPN list processing in Browning et al. does not correspond to "indication in a virtual memory data structure associated with the process

that the virtual address space, previously available to the process, is no longer valid"

In respond to Applicant's argument as stated above, Browning clearly teaches providing a flag to indicate whether virtual memory is removed in progress (step 834, figure 8 and col. 8 lines 32-44) and reinitializing real page number RPN entry and mark entry as valid when memory remove in progress flag is not set such that the memory remove in progress flag provides an indication in a virtual memory data structure associated with the process. Also, Browning also teaches that the real page number (RPN) list includes pre-translations for a particular set of virtual addresses so that each RPN list includes a list of different set of virtual addresses (col. 3 line 60 through col. 4 line 13). Note Browning also teaches that the pre-translations are stored in an RPN list which is stored with the buffer memory descriptor (col. 7 lines 15-16) and a transient flag is set in the buffer descriptor for determining whether virtual memory is removed in progress (col. 7 line 50 through col. 8 line 44). Thus, the RPN list as taught by Browning can be considered as the virtual memory data structure, and the transient flag as taught by Browning can be read on the claimed limitations of "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid".

(2) In-progress flag in Browning et al. does not correspond to "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid"

In respond to Applicant's argument as stated above, Browning clearly teaches the memory-remove-in-progress flag is part of a virtual memory data structure because the memory-remove-in-progress flag is set in the buffer descriptor which is stored with RPN list (col. 7 lines 15-16 and col. 8 lines 33-34). Note Browning also teaches that each RPN list including a list of different sets of virtual addresses. Thus, one skill in the art would recognize the memory-remove-in progress flag is part of a virtual memory data structure and the flag has affect a particular process as required by claim 1.

(3) Browning et al. as a whole does not teach "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid"

As noted above, Examiner has provided rationale for how Browning teaches the elements of the claim are disclosed such that the memory-remove-in-progress flag is set in the buffer descriptor which is stored with RPN list (col. 7 lines 15-16 and col. 8 lines 33-34). Therefore, the broad claimed limitations as recited in claim 1 are read by the combination of Armilli and Browning.

(4) The combination as a whole does not teach "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid"

As noted above, Browning teaches the claimed features as recited in claim 1. Thus, the combination of Armilli and Browning teaches all the claimed limitations as recited in claim 1, a *prima facie* case of obviousness has been made, and the rejection should be sustained.

b. The proposed combination does not teach "the indication is triggered by detection that the physical address space that was being used by processes associated with the device has been released"

(1) Checking the memory-move-in-progress flag in Browning et al. does not correspond to "the indication is triggered by detection that the physical address space that was being used by processes associated with the device has been released"

In respond to Applicant's argument as stated above, examiner respectively disagrees because Browning clearly teaches to trigger an indication by detection that the physical address space that was being used by processes associated with the device has been released, i.e., set memory remove in progress flag after determination of RPN entry for the virtual memory page is invalid (see steps 824-834 and col. 8 lines 18-44). Thus, the action that

occurs in Browning, if the RPN entry for the virtual memory page is detected as invalid due to the physical address space that was being used by the processes associated with the device has been released, the memory-remove-in-progress flag is triggered or set.

(2) In-progress flag in Browning et al. does not correspond to "the indication is triggered by detection that the physical address space that was being used by processes associated with the device has been released"

In response to Applicant's argument that the memory remove operation as taught by Browning is not the same as release of physical address space as describe in claim 1, examiner respectfully disagrees because the claimed language fails to specifically define how to release of physical address space such that one skill in the art would recognize the teaching of Browning removal of real pages of memory (col. 9 lines 4-10) being read on the claimed limitation of release of physical address space. Note Browning also teaches the limitations of "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid" and "trigger an indication by detection that the physical address space that was being used by processes associated with the device has been released" as stated above. Thus, Browning teaches the claimed features.

(3) The combination as a whole does not teach "an indication in a virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for use by the process"

Examiner has explained in accordance with above sections on why Browning teaches this feature. Since the references disclose these features, a *prima facie* case of obviousness has been made, and the rejection should be sustained.

c. Conclusion

As explained above, the proposed combination of Armilli in view of Browning teaches at least the features noted above and recited in claim 1. Therefore, a *prima facie* case establishing an obviousness rejection has been made, and the rejection should be sustained.

2. Independent claim 8

a. The proposed combination does not teach "register by providing an indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

(1) RPN list processing in Browning et al. does not correspond to "indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

In respond to Applicant's argument as stated above, Browning clearly teaches providing a flag to indicate whether virtual memory is removed in progress (step 834, figure 8 and col. 8 lines 32-44) and reinitializing real page number RPN entry and mark entry as valid when memory remove in progress flag is not set such that the memory remove in progress flag provides an indication in a virtual memory data structure associated with the process. Also, Browning also teaches that the real page number (RPN) list includes pre-translations for a particular set of virtual addresses so that each RPN list includes a list of different set of virtual addresses (col. 3 line 60 through col. 4 line 13). Note Browning also teaches that the pre-translations are stored in an RPN list which is stored with the buffer memory descriptor (col. 7 lines 15-16) and a transient flag is set in the buffer descriptor for determining whether virtual memory is removed in progress (col. 7 line 50 through col. 8 line 44). Thus, the RPN list as taught by Browning can be considered as the virtual memory data structure, and the transient flag as taught by Browning can be read on the claimed limitations of "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid".

(2) In-progress flag in Browning et al. does not correspond to "indication in a virtual memory data structure associated with the process

that the virtual address space, previously available to the process, is no longer valid"

In respond to Applicant's argument as stated above, Browning clearly teaches the memory-remove-in-progress flag is part of a virtual memory data structure because the memory-remove-in-progress flag is set in the buffer descriptor which is stored with RPN list (col. 7 lines 15-16 and col. 8 lines 33-34). Note Browning also teaches that each RPN list including a list of different sets of virtual addresses. Thus, one skill in the art would recognize the memory-remove-in progress flag is part of a virtual memory data structure and the flag has affect a particular process as required by claim 8.

(3) Browning et al. as a whole does not teach "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid"

As noted above, Examiner has provided rationale for how Browning teaches the elements of the claim are disclosed such that the memory-remove-in-progress flag is set in the buffer descriptor which is stored with RPN list (col. 7 lines 15-16 and col. 8 lines 33-34). Therefore, the broad claimed limitations as recited in claim 8 are read by the combination of Armilli and Browning.

(4) The combination as a whole does not teach "indication in a virtual memory data structure associated with the process that the virtual

address space, previously available to the process, is no longer available to the process"

As noted above, Browning teaches the claimed features as recited in claim 1. Thus, the combination of Armilli and Browning teaches all the claimed limitations as recited in claim 1, a *prima facie* case of obviousness has been made, and the rejection should be sustained.

b. The proposed combination does not teach "to register is triggered by detection that the physical address space that was being used by processes associated with the device has been released"

(1) Checking the memory-move-in-progress flag in Browning et al. does not correspond to "the indication is triggered by detection that the physical address space that was being used by processes associated with the device has been released"

In respond to Applicant's argument as stated above, examiner respectively disagrees because Browning clearly teaches to trigger an indication by detection that the physical address space that was being used by processes associated with the device has been released, i.e., set memory remove in progress flag after determination of RPN entry for the virtual memory page is invalid (see steps 824-834 and col. 8 lines 18-44). Thus, the action that occurs in Browning, if the RPN entry for the virtual memory page

is detected as invalid due to the physical address space that was being used by the processes associated with the device has been released, the memory-remove-in-progress flag is triggered or set.

(2) In-progress flag in Browning et al. does not correspond to "to register is triggered by detection that the physical address space that was being used by processes associated with the device has been released"

In response to Applicant's argument that the memory remove operation as taught by Browning is not the same as release of physical address space as describe in claim 1, examiner respectfully disagrees because the claimed language fails to specifically define how to release of physical address space such that one skill in the art would recognize the teaching of Browning removal of real pages of memory (col. 9 lines 4-10) being read on the claimed limitation of release of physical address space. Note Browning also teaches the limitations of "indication in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid" and "to register is triggered by detection that the physical address space that was being used by processes associated with the device has been released" as stated above. Thus, Browning teaches the claimed features.

(3) The combination as a whole does not teach "an indication in a virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for use by the process"

Examiner has explained in accordance with above sections on why Browning teaches this feature. Since the references disclose these features, a *prima facie* case of obviousness has been made, and the rejection should be sustained.

c. Conclusion

As explained above, the proposed combination of Armilli in view of Browning teaches at least the features noted above and recited in claim 8. Therefore, a *prima facie* case establishing an obviousness rejection has been made, and the rejection should be sustained.

3. Independent Claim 13

a. The proposed combination does not teach "means for unmapping a virtual address space for the process...in a manner which does not violate semantics for an operating system of the computing device"

In respond to Applicant's argument that the proposed combination does not teach "means for unmapping a virtual address space for the process…in a manner which does not violate semantics for an operating system of the computing device", it appears that Armilli teaches each

virtual address space is translated by a page table translation into real address space (see col. 6 lines 3-39). Note Armilli also teaches to remove a particular module so that a move engine provides a virtualization function of the physical memory to perform data transfer between modules of physical memory as reconfiguration (col. 7 lines 16-31). Thus, the virtual memory address space for the process as taught by Armilli needs to be unmapped when the particular module is removed. Note Armilli also teaches the processor's move engine works in conjunction with the associated mapping engine to take the associated memory module offline, read as un-mapping a virtual address space, prior to its physically removal, read as when the removable memory mappable device associated with the process is logically disconnected, such that the memory module can be removed in physical memory without the operating system having to direct and control the reconfiguration of physical memory to accomplish the physical memory chance, read as for a process in a manner which does not violate semantics for an operating system of the computing device (abstract and col. 7 line 32 through col. 9 line 10). Therefore, the proposed combination of Armilli in view of Browning does teach at least the features noted above and recited in claim 13

4. Independent claim 19

a. The proposed combination does not teach "providing an indication in the virtual memory data structure for the process that a virtual address space is no longer available for use by the process"

(1) RPN list processing in Browning et al. does not correspond to "indication in the virtual memory data structure for the process that a virtual address space is no longer available for use by the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (1) in independent claim 1 under section **a** (pages 14-15 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

(2) In-progress flag in Browning et al. does not correspond to "indication in the virtual memory data structure for the process that a virtual address space is no longer available for use by the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (2) in independent claim 1 under section **a** (page 16 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

(3) Browning et al. as a whole does not teach "indication in the virtual memory data structure for the process that a virtual address space is no longer available for use by the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (3) in independent claim 1 under section **a** (page 16 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

(4) The combination as a whole does not teach "indication in the virtual memory data structure for the process that a virtual address space is no longer available for use by the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (4) in independent claim 1 under section **a** (page 17 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

b. The proposed combination does not teach "as triggered by detection of a physical address space used by the process being released and when the object is removed from physical memory"

(1) Checking the memory-move-in-progress flag in Browning et al. does not correspond to "as triggered by detection of a physical address space used by the process being released and when the object is removed from physical memory"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (1) in independent claim 1 under section **b** (pages 17-18 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

(2) In-progress flag in Browning et al. does not correspond to "as triggered by detection of a physical address space used by the process being released and when the object is removed from physical memory"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (2) in independent claim 1 under section **b** (page 18 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

(3) The combination as a whole does not teach "an indication in a virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for use by the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (3) in independent claim 1 under section **b** (page 19 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 19 are read by the combination of Armilli and Browning.

c. Conclusion

As explained above, the proposed combination of Armilli in view of Browning teaches at least the features noted above and recited in claim 19. Therefore, a *prima facie* case establishing an obviousness rejection has been made, and the rejection should be sustained.

5. Independent claim 22

a. The proposed combination does not teach "registering an indication in a virtual memory data structure for the process that the virtual address space is not available to the process"

(1) RPN list processing in Browning et al. does not correspond to "indication in a virtual memory data structure for the process that the virtual address space is not available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are

disclosed as the same reasons as stated under item (1) in independent claim 8 under section **a** (pages 19-20 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 22 are read by the combination of Armilli and Browning.

(2) In-progress flag in Browning et al. does not corresponding to "indication in a virtual memory data structure for the process that the virtual address space is not available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (2) in independent claim 8 under section **a** (pages 20-21 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 22 are read by the combination of Armilli and Browning.

(3) Browning et al. as a whole does not teach "indication in a virtual memory data structure for the process that the virtual address space is not available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (3) in independent claim 8 under section **a** (page 21 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 22 are read by the combination of Armilli and Browning.

(4) The combination as a whole does not teach "indication in a virtual memory data structure for the process that the virtual address space is not available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (4) in independent claim 8 under section **a** (pages 21-22 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 22 are read by the combination of Armilli and Browning.

b. The proposed combination does not teach "[registering an indication] at the release of the physical address space used by the process and before the process has released the virtual address space"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated in independent claim 8 under section **b** (pages 22-24 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 22 are read by the combination of Armilli and Browning.

c. Conclusion

As explained above, the proposed combination of Armilli in view of Browning teaches at least the features noted above and recited in claim 22. Therefore, a *prima facie* case establishing an obviousness rejection has been made, and the rejection should be sustained.

6. Independent claim 23

a. The proposed combination does not teach "registering an indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

(1) RPN list processing in Browning et al. does not correspond to "indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (1) in independent claim 1 under section **a** (pages 14-15 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 23 are read by the combination of Armilli and Browning.

(2) In-progress flag in Browning et al. does not correspond to "indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (2) in independent claim 1 under section **a** (page 16 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 23 are read by the combination of Armilli and Browning.

(3) Browning et al. as a whole does not teach "indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (3) in independent claim 1 under section **a** (page 16 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 23 are read by the combination of Armilli and Browning.

(4) The combination as a whole does not teach "indication in a virtual memory data structure for the process that the virtual address space is no longer available to the process"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated under item (4) in independent claim 1 under section **a** (page 17 of instant examiner's answer). Therefore, the broad

claimed limitations as recited in claim 23 are read by the combination of Armilli and Browning.

b. The proposed combination does not teach "[registering an indication] at the release of the physical address space used by the process and before the process has released the virtual address space"

In respond to Applicant's argument as stated above, Examiner has provided rational for how Browning teaches the elements of the claim are disclosed as the same reasons as stated in independent claim 1 under section **b** (pages 17-19 of instant examiner's answer). Therefore, the broad claimed limitations as recited in claim 23 are read by the combination of Armilli and Browning.

c. Conclusion

As explained above, the proposed combination of Armilli in view of Browning teaches at least the features noted above and recited in claim 23. Therefore, a *prima facie* case establishing an obviousness rejection has been made, and the rejection should be sustained.

7. **Dependent claims 2-7, 9-12, 14-18, and 20-21**

As explained above, dependent claims 2-7, 9-12, 14-18, and 20-21 are rejected for at least the reason set forth above from independent claims 1, 8, 13,

19, 22, and 23, respectively. Therefore, the rejection in claims 2-7, 9-12, 14-18, and 20-21 should be sustained.

Conclusion

In view of the forgoing discussion, it is respectfully submitted that all pending claims 1-23 are reject under the cited reference. A reconsideration and direct passage to affirm the rejection of all pending claims are respectfully requested.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Zhuo H Li/

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